CLAIMS

1. A method of making a recessed gate field effect power MOS device, the method comprising:

forming a substrate (20) including first and second doped layers (24, 26) of first and second opposite dopant polarities to define a body region adjoining an upper surface of the substrate and an underlying drain region;

forming a trenching protective layer (30) on the upper surface (28) of the substrate;

masking and patterning the trenching protective layer to define an exposed first area (46) and a protected second area of the upper surface of the substrate demarcated by opposite sidewalls of the trenching protective layer;

forming sidewall spacers (44) having inner surfaces (48) contacting opposite sidewalls of the trenching protective layer (30) and outer surfaces (47) spaced a predetermined spacing (54) from the sidewalls of the trenching protective layer;

forming in the first area (46) of the substrate, between the outer surfaces (47) of the sidewall spacers (44) , a first trench (50) having sidewalls aligned relative to the outer surfaces (47) of the sidewall spacers and extending at least through the layer (26) defining the body region to a bottom wall at least a predetermined depth (56) from the upper surface of the substrate;

forming a gate oxide layer (60) on the first trench sidewalls;

filling the first trench with polysilicon (62) to a level (64) spaced between the upper surface of the substrate and a top surface of the trenching protective layer (30);

applying a protective layer (68) selectively over the polysilicon (62) filled into the first trench, between the sidewall spacers (44) and in contact with the outer surfaces (47) of the sidewall spacers;

removing the trenching protective layer to expose the second area of the upper surface (28') of the substrate between the inner surfaces (48) of the sidewall spacers;

doping the second area of the upper surface (28') of the substrate between the gate oxide layer (60) on the trench sidewalls with dopant of said second dopant polarity to form a source region (72) atop the body region (26');

forming, in the second area of the substrate (28') between the inner surfaces (48) of the sidewall spacers (44), a second trench (80) having sidewalls aligned relative to the inner surfaces of the sidewall spacers and extending through the layer (72) defining the source region to a bottom wall in the body region (26") of the substrate; and

depositing a source conductive layer (94) in the second trench in contact with the source region and the body region;

the second trench (80) through the source region and body region defining vertically-oriented source and body layers (86, 90) stacked along the gate oxide layer (60) on opposite sidewalls of the second trench (80) and having a lateral thickness (88) established by the predetermined spacing of the inner and outer surfaces of the sidewall spacers.

2. A method according to claim 1 in which the body layer (90) is sized to a lateral thickness (88) less than a vertical height (83) thereof.

3. A method according to claim 1 in which the body layer (90) is sized to a lateral thickness (88) less than 1 μm.

4. A method according to claim 3 in which the vertically-oriented body layer (90) is doped to a first doping concentration and a laterally-extending portion of the body region (26") is doped to a second doping concentration greater than the first doping concentration.

5. A method according to claim 1 including forming an insulative layer (68) between the sidewall spacers (44) over the source conductor (94) to electrically isolate the gate conductor (62) from the source conductor.

6. A method according to claim 1 in which the second trench is formed to a depth (82) such that the source conductive layer (94) extends vertically along both the source and body layers (86, 90) to form a short across a PN junction formed therebetween and contacts a laterally-extending upper surface of the body region (26) at a position spaced below the PN junction.

7. A method according to claim 1 in which substrate (20) includes a base layer (122) underlying the first doped layer (24) and doped with a dopant of said first polarity to a doping concentration greater than a doping concentration of the first doped layer (24) to form a three-layer power MOSFET.

8. A method according to claim 7 in which the first trench is formed to a depth (156) extending into the base layer and the gate oxide layer is formed in a first portion (160A) having first thickness in a lower portion of the trench and a second portion (160B) having a second thickness in an upper portion of the trench, the first thickness being greater than the second thickness.

9. A method according to claim 1 in which substrate (20) includes a base layer (22) underlying the first doped layer (24) and doped with a dopant of said second polarity to define a four-layer PNPN device.

10. A method according to claim 9 in which the first trench is formed to a depth (256) within the first layer spaced above the base layer and the gate oxide layer is formed in a first portion (260A) having a first thickness in a lower portion of the trench and a second portion (260B) having a second thickness in an upper portion of the trench, the first thickness being greater than the second thickness.

11. A method according to claim1 in which:

the first trench is formed to a first depth;

a first gate oxide layer (160A, 260A) is formed with a first thickness;

a filler material is filled into the trench to a second depth less than the first depth;

a portion of the first gate oxide layer is removed above the filler material;

a second gate oxide layer (160B, 260B) is formed with a second thickness; and

the trench is filled above said second depth with a conductive gate material.

12. A method according to claim11 in which the filler material includes polysilicon and the second gate oxide layer (160B, 260B) is formed over the polysilicon.

13. A method according to claim11 in which the filler material includes

photoresist and the photoresist is removed before the second gate oxide layer is formed.

14. A method according to claim1 in which the trenching protective layer comprises a thin oxide layer (32) formed atop the upper substrate surface, a polysilicon layer deposited on the thin oxide layer, and a thick oxide layer (36) deposited on the polysilicon layer.

15. A method according to claim1 in which the trenching protective layer (330) comprises a first oxide layer (32) formed atop the upper substrate surface, a first polysilicon layer (34, 334) deposited on the first oxide layer, a second oxide layer (36, 336) formed on the first polysilicon layer; and a second polysilicon layer (338) deposited on the second oxide layer.

16. A method according to claim1 in which the first trench and the gate oxide layer and gate conductor within the first trench define a gate structure which is laterally patterned in two dimensions to define an interconnected matrix enclosing a plurality of islands, each island being formed with said second trench extending into a central portion thereof and containing a downward extending finger of source conductor surrounded by a portion of the source and body layers (86, 90) including a vertical channel having a width defined in each island by a perimeter of the island.

17. A method according to claim 16 in which the body layer (90) is sized to a lateral thickness (88) proportionate to the predetermined spacing (52) between the inner surfaces (48) and outer surfaces (47) of the sidewall spacers (44).

18. A method according to claim1 including forming at least two of said first trenches at a predetermined lateral spacing and forming said second trench between the first trenches at a spacing therefrom determined by said predetermined spacing (52) between the inner and outer surfaces of the sidewall spacers, the first trenches each containing the gate oxide layer and gate conductor, the source conductor extending into the second trench and contacting the vertically oriented source and body layers (86, 90) on opposite sides thereof.

19. A method according to claim 18 in which the body layer (90) is sized to a lateral thickness (88) proportionate to the predetermined spacing (52) between the inner surfaces (48) and outer surfaces (47) of the sidewall spacers (44).

20. A method according to claim 1 in which the body layer (90) is sized to a lateral thickness (88) proportionate to the predetermined spacing (52) between the inner surfaces (48) and outer surfaces (47) of the sidewall spacers (44).

21. A recessed gate field effect power MOS device having a vertically oriented channel comprising:

a semiconductor substrate (20) including first and second laterally-extending layers (24, 26) of first and second opposite polarity dopants defining a body layer (26) and an underlying drain layer (24);

a first trench (50) having sidewalls extending depthwise from an upper surface (28) of the substrate at least through the body layer to a bottom wall at a predetermined depth from the upper surface of the substrate;

a gate oxide layer (60) on the trench sidewalls and bottom wall;

a first, gate conductor (62) filling the first trench depthwise to at least

an elevation of the upper surface of the substrate and contacting the gate oxide layer on the trench sidewalls;

a vertically oriented layer (86, 90) of semiconductor substrate extending upward along the gate oxide layer (60) on opposite sides of the first trench from the body layer to the upper surface of the substrate; and

a vertically-extending source conductor (94) contacting the vertically oriented layer on a side opposite the gate oxide layer and gate conductor;

the vertically oriented layer including a first vertical layer portion (90) contiguous with the body layer doped with said first polarity dopant to define an active body region including a vertical channel and a second vertical layer portion (86) atop the first vertical layer portion (90) and forming a PN junction therewith;

the second vertical layer portion being doped with said second polarity dopant to form a source region contacting the active body region, and the source conductor electrically shorting the source region to the active body region across the PN junction.

22. A recessed gate field effect power MOS device according to claim 21 in which the first vertical layer portion has a lateral thickness (88) less than a vertical height (83) thereof.

23. A recessed gate field effect power MOS device according to claim ~~21~~ 1 in which the first vertical layer portion has a lateral thickness (88) less than 1 μm.

24. A recessed gate field effect power MOS device according to claim 23 in which the first vertical layer portion (90) is doped to a first doping concentration and the laterally-extending body layer (26) is doped to a

second doping concentration greater than the first doping concentration.

25. A recessed gate field effect power MOS device according to claim 21 including a vertically-oriented sidewall spacer (44) extending upward from the the upper surface of the substrate atop the vertically oriented layer .

26. A recessed gate field effect power MOS device according to claim 25 including one of said vertically oriented layers on each side of the trench , each having one of said vertically-oriented sidewall spacer thereon, and an insulative layer (68) extending laterally between atop the sidewall spacers over the gate conductor .

27. A recessed gate field effect power MOS device according to claim 21 including means (44, 68, 60) defining an insulative layer electrically isolating the gate conductor from the source conductor.

28. A recessed gate field effect power MOS device according to claim 21 in which vertically-extending source conductor (94) contacts the laterally-extending body layer at a position spaced below the PN junction.

29. A recessed gate field effect power MOS device according to claim 28 in which the first vertical layer portion is doped to a first doping concentration defining a threshhold voltage of the channel and the laterally-extending body layer is doped to a second doping concentration greater than the first doping concentration.

30. A recessed gate field effect power MOS device according to claim 34 ~~21~~ in which the first trench and the gate oxide layer and gate conductor within

the trench form a gate structure which is laterally patterned in two dimensions to define an interconnected matrix enclosing a plurality of islands each containing a downward extending finger of source conductor surrounded by a portion of the active body region including said vertical channel, the channel having a width defined in each island by a perimetral length of the island.

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31. A recessed gate field effect power MOS device according to claim 34 21 including at least two of said first trenches spaced laterally apart with two of said vertically oriented layers of semiconductor substrate defining a second trench between the first trenches, the first trenches containing the gate oxide layer and gate conductor, said source conductor extending into the second trench and contacting the vertically oriented layer on opposite sides thereof.

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32. A recessed gate field effect power MOS device according to claim 34 21 in which the substrate includes a base layer of said first polarity dopant such that the device defines an alternating PNPN four-layer structure wherein the body layer defines a base of an upper bipolar transistor and a collector of a lower bipolar transistor.

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33. A recessed gate field effect power MOS device according to claim 34 21 in which the first trench has a predetermined depth (156, 256) within the first layer and the gate oxide layer includes a first portion (160A, 260A) having a first thickness in a lower portion of the trench and a second portion (160B, 260B) having a second thickness in an upper portion of the trench, the first thickness being greater than the second thickness.

figs. 20, 21

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